REMARKS

Claims 1-23 are pending in the present application. Applicants have amended Claims 5, 8, 12, 16 and 23 herewith. Reconsideration of the claims is respectfully requested.

I. Claim Objection

The Examiner objected to Claim 23, stating that Claim 23 recites the limitations "first determination means" in page 12, lines 3 and 6 and therefore requires appropriate correction. Applicants have reviewed both Claim 23 and the passage cited at page 12, lines 3 and 6. Neither Claim 23 nor the passage cited at page 12, lines 3 and 6 include "first determination means" terminology. Therefore, Applicants are unclear as to the specific basis for the objection to Claim 23. Further clarification is requested.

II. 35 U.S.C. § 112, Second Paragraph

The Examiner rejected Claims 5-6 and 8-22 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention. This rejection is respectfully traversed.

With respect to Claims 5, 8 and 16, the Examiner states "the physical processor" is vague and unclear since it does not specify whether it is referring to the first or the second physical processor. Applicants have amended such claims accordingly to clarify which physical processor is being referred to.

With respect to Claims 12 and 23, the Examiner states "the active number" has insufficient antecedent basis. Applicants have amended such claims accordingly to provide proper antecedent basis.

Therefore the rejection of Claims 5-6 and 8-22 under 35 U.S.C. § 112, second paragraph has been overcome.

III. **35 U.S.C. § 102, Anticipation**

The Examiner rejected Claims 1, 2, 12, 13 and 23 under 35 U.S.C. § 102(b) as being anticipated by Applicants' admitted prior art. This rejection is respectfully traversed.

Per 35 U.S.C. § 102(b), a person shall be entitled to a patent unless—

> the invention was patented or described in a **printed publication** in this or a foreign country or in public use or on sale in this country, **more than one year** prior to the date of the application for patent in the United States.

Applicants discussion of background art in the present patent application does *not* establish either (i) that the claimed invention was patented or described in a printed publication in this or a foreign country, (2) that the claimed invention was in public use or on sale in this country, or (3) that either (1) or (2) occurred more than one year prior to the filing data of the present patent application. Therefore, the Examiner has failed to establish that Claims 1, 2, 12, 13 and 23 were patented or described in a *printed publication* in this or a foreign country or in public use or on sale in this country, *more than one year* prior to the date of the application for patent in the United States, and thus the rejection of such claims under 35 U.S.C. § 102(b) is shown to be in error.

Further with respect to Claim 1, Applicants show that the background section of the present application does not teach steps of (i) determining whether a *second logical processor* on the first physical processor is busy *if the first logical processor* is idle; and (ii) relinquishing resources of the first physical processor *to the second logical processor if the second logical processor is busy*. The background section merely states that an idle processor checks for threads to acquire from another run queue (page 3, lines 7-15). There is no teaching of a conditional check of whether a *second* logical processor is *busy*, the condition for such check being whether the *first* logical processor is *idle*. Claim 1 expressly recites first and second logical processors on a physical processor, and an alleged teaching of a single processor stealing threads from a thread queue does not teach or otherwise disclose the claimed plurality of logical processors and the associated

actions recited in Claim 1, such as determining whether a *second* logical processor on the first physical processor *is busy if the first logical processor is idle*, or relinquishing resources of the first physical processor to the second logical processor *if the second logical processor is busy*.

This conditional check of whether a second logical processor is busy if the first logical processor is idle is shown in the preferred embodiment at FIG 3, element 310, and occurs after a determination has been made by block 304 that the first logical processor is idle (as described by Applicants at Specification page 11, line 14 – page 12, line 8). In contrast, the discussion in the background section merely states an ability to steal/acquire a thread (from a thread queue) by a processor when such processor becomes idle. This stealing/acquiring of a thread from a thread queue is not conditioned upon the status of any other processor, either physical or logical. Claim 1 expressly cites such conditional status of another processor, and in particular recites determining whether a *second logical processor* on the first physical processor is busy if the *first logical processor* is idle; and relinquishing resources of the first physical processor to the second logical processor if the second logical processor is busy. For a prior art reference to anticipate in terms of 35 U.S.C. 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990) (emphasis added by Applicants). Thus, even assuming arguendo that the background section of the present application is prior art (which, as Applicants have shown above it is not), every element of the claimed invention is *not* identically shown in this background section and thus Claim 1 is further shown to have been erroneously rejected under 35 U.S.C. 102(b).

With respect to Claims 2, 12, 13 and 23, Applicants initially traverse for similar reasons to those given above with respect to Claim 1.

Further with respect to Claim 2 (and similarly for Claim 13), Applicants show that the background section of the present application does not teach "wherein the step of determining *whether the first logical processor is idle* comprises (i) determining whether the first logical processor is running a current job; *and* (ii) determining whether a first run queue corresponding to the first logical processor is empty if the first logical processor is not running a current job, wherein the first logical processor is idle if the first run queue is empty" (emphasis added by Applicants). In rejecting Claim 2, the Examiner states that

these two steps are taught in the present application at page 3, lines 11-13. Applicants show that there, the present application states:

> "When a logical processor becomes idle and there are no threads waiting in the run queue, the processor checks for threads to "steal," or acquire from another logical processor's run queue."

As can be seen, this passage states that if two conditions are met (the logical processor is idle; there are no threads waiting in the run queue), a check is made for threads to steal or acquire from another run queue. There is no detail provided as to *how* the determination is made as to whether the processor is idle – only a statement that "When a logical processor *becomes* idle" (emphasis added by Applicants). In contrast, Claim 2 is a further refinement of the step of determining whether a processor is idle, and such processor idle determination comprises two steps: (i) determining whether the first logical processor is running a current job; *and* (ii) determining whether a first run queue corresponding to the first logical processor is empty if the first logical processor is not running a current job, wherein the first logical processor is idle if the first run queue is empty. A simple statement of "When a processor is idle" per page 3 lines 11-13 of the present Application does not teach *how* such idle determination is made, and in particular does not teach that idle determination is made comprising steps of (i) determining whether the first logical processor is running a current job; *and* (ii) determining whether a first run queue corresponding to the first logical processor is empty if the first logical processor is not running a current job, wherein the first logical processor is idle if the first run queue is empty. Thus, Claim 2 (and similarly for Claim 13) is further shown to have been erroneously rejected under 35 U.S.C. 102(b), as every claimed element is not identically shown in a single reference.

Therefore, the rejection of Claims 1, 2, 12, 13 and 23 under 35 U.S.C. § 102 has been overcome.

IV. **35 U.S.C. § 103, Obviousness**

A. The Examiner rejected Claims 3-6 and 14-17 under 35 U.S.C. § 103 as being unpatentable over Applicants' admitted prior art. This rejection is respectfully traversed.

Per 35 U.S.C. § 103(a), a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains (emphasis added by Applicants).

Applicants' background art discussion is not 'prior art' that can properly be used in a 35 U.S.C. § 103(a) rejection, for similar reasons to those listed above with respect to the rejection of Claims 1, 2, 12, 13 and 23 pertaining to the background section of the present application not being a valid 35 U.S.C. 102(b) reference.

Applicants further traverse the rejection of Claims 3-6 and 14-17 for similar reasons to those further reasons given above with respect to Claim 1, and show that even assuming arguendo that Applicants' background section is prior art (which Applicants urge it is not), there is no teaching or suggestion in such background section of (i) determining whether a second logical processor on the first physical processor is busy if the first logical processor is idle; and (ii) relinquishing resources of the first physical processor to the second logical processor if the second logical processor is busy (which steps are expressly recited in Claim 1). Thus, Claims 3-6 and 14-17 are further shown to have been erroneously rejected under 35 U.S.C. § 103.

Still further with respect to Claims 3 and 4 (and similarly for Claims 14 and 15) and for similar reasons to those further reasons given above with respect to Claim 2 (of which Claims 3 and 4 depend upon), Applicants show that the cited background section of the present application does not teach or suggest "wherein the step of determining whether the first logical processor is idle comprises (i) determining whether the first logical processor is running a current job; and (ii) determining whether a first run queue corresponding to the first logical processor is empty if the first logical processor is not running a current job, wherein the first logical processor is idle if the first run queue is empty" (which is expressly recited in Claim 2). Thus, Claims 3 and 4 (and similarly for

Claims 14 and 15) are further shown to have been erroneously rejected under 35 U.S.C. § 103.

B. The Examiner rejected Claims 7, 8 and 18-19 under 35 U.S.C. § 103 as being unpatentable over Applicants' admitted prior art in view of Konig (US Pat. Application Publication 2002/0133530). This rejection is respectfully traversed.

Applicants traverse the rejection of Claims 7, 8 and 18-19 for reasons given above with respect to the 35 U.S.C. 103(a) rejection of Claims 3-6 and 14-17 pertaining to invalid prior art being used in the claim rejection. Thus, Claims 7, 8 and 18-19 are shown to have been erroneously rejected under 35 U.S.C. § 103.

Applicants further traverse the rejection of Claims 7 and 8 (and similarly for Claims 18-19) for the further reasons given above with respect to Claim 1 (of which Claims 7 and 8 depend upon), and show that none of the cited references teach or suggest the steps of (i) determining whether a second logical processor on the first physical processor is busy if the first logical processor is idle; and (ii) relinquishing resources of the first physical processor to the second logical processor if the second logical processor is busy (which is expressly recited in Claim 1). Thus, Claims 7, 8 and 18-19 are further shown to have been erroneously rejected under 35 U.S.C. § 103.

C. The Examiner rejected Claims 9-11 and 20-22 under 35 U.S.C. § 103 as being unpatentable over Applicants' admitted prior art in view of Konig (US Pat. Application Publication 2002/0133530), as applied to claims 1, 8, 12 and 19 above, and further in view of Welland et al. (US 5,247,677). This rejection is respectfully traversed.

Applicants initially traverse the present rejection for similar reasons to those given above in the discussion of Claims 3-6 and 14-17 and valid prior art, and urge that the present application is not valid prior art for a 35 U.S.C. 103 rejection.

Applicants further traverse the rejection of Claims 9-11 (and similarly for Claims 20-22) for similar reasons to those further reasons given above with respect to Claim 1 (of which Claims 9-11 ultimately depend upon), and show that even assuming arguendo that Applicants' background section is prior art (which Applicants urge it is not), there is no teaching or suggestion in such background section of (i) determining whether a second

logical processor on the first physical processor is busy if the first logical processor is idle; and (ii) relinquishing resources of the first physical processor to the second logical processor if the second logical processor is busy (as expressly recited in Claim 1). Thus, Claims 9-11 (and similarly for Claims 20-22) are further shown to have been erroneously rejected under 35 U.S.C. § 103.

Applicants further traverse such rejection of Claims 10 and 11 (and similarly for Claims 21 and 22) by showing that none of the cited references teach or suggest the claimed step of "raising the priority of the first logical processor after the predetermined period of time". In rejecting Claim 10, the Examiner states that Welland teaches that task 24c current priority is raised from 12 to 15 making task 24c the highest priority which is to be scheduled for execution and at the end of one time slice, the current priority of task 24c would be *decremented*. Claim 10 recites just the opposite – that the priority is *raised* after the predetermined period of time. Thus, the Examiner has failed to establish a prima facie showing of obviousness with respect to Claim 10[1], and the burden has not shifted to Applicants to rebut the obviousness rejection[2]. Thus, Claims 10 and 11 (and similarly for Claims 21 and 22) are further shown to have been erroneously rejected under 35 U.S.C. § 103.

Still further with respect to Claim 11 (and similarly with respect to Claim 22), none of the cited references teach or suggest the claimed step of "dispatching a job to the first logical processor in response to the raised priority". Because the cited Welland reference teaches that the priority is *decremented* after the predetermined period of time, the job would not be dispatched *in response to the raised priority* as the priority is not raised, but instead is lowered. Thus, Claim 11 (and similarly for Claim 22) is still further shown to have been erroneously rejected.

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[1] In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). To establish prima facie obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. MPEP 2143.03. *See also, In re Royka*, 490 F.2d 580 (C.C.P.A. 1974).

[2] Only if that burden is met, does the burden of coming forward with evidence or argument shift to the applicant. *In re Oetiker*, supra.

D. Therefore, the rejection of Claims 3-11 and 14-22 under 35 U.S.C. § 103 has been overcome.

V. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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